CLAIMS

What is claimed is:

1. An electronic fuse, comprising a logic gate and at least one nonvolatile memory element, said at least one nonvolatile memory element configured to be programmed to a memory value capable of causing an input to said logic gate to settle to a predetermined state as a power-up or a reset signal is applied to the fuse.

2. The electronic fuse of Claim 1, wherein said nonvolatile memory element comprises a floating-gate transistor having a floating gate, an amount of charge on the floating gate determining said memory value.

3. The electronic fuse of Claim 2, wherein said nonvolatile memory element further comprises a first capacitor having a first plate in common with the floating gate of said floating-gate transistor.

4. The electronic fuse of Claim 1, wherein said nonvolatile memory element comprises a nonvolatile memory element manufactured in a MOS fabrication process.

5. The electronic fuse of Claim 2, wherein said floating-gate transistor is a MOS device.

6. The electronic fuse of Claim 1, wherein said nonvolatile memory element uses a mechanism selected from the group consisting of: magnetoresistive, ferroelectric, phase-change, and dielectric, for nonvolatile information storage.

7. The electronic fuse of Claim 2, wherein the amount of charge on the floating gate may be changed using Fowler-Nordheim tunneling.

8. The electronic fuse of Claim 2, wherein the amount of charge on the floating gate may be changed using hot-electron injection.

9. The electronic fuse of Claim 2, wherein the amount of charge on the floating gate may be changed using direct tunneling.

10. The electronic fuse of Claim 2, wherein the amount of charge on the floating gate may be changed using hot-hole injection.

11. The electronic fuse of Claim 2, wherein the amount of charge on the floating gate may be changed using ultraviolet radiation exposure.

12. The electronic fuse of Claim 2, wherein said nonvolatile memory element further comprises a first capacitor having a first plate in common with the floating gate of said floating-gate transistor.

13. The electronic fuse of Claim 12, wherein the nonvolatile memory element further comprises a second capacitor having a first plate in common with the floating gate of said floating-gate transistor.

14. A master-slave electronic fuse, comprising:

a master fuse having a master latch and a nonvolatile memory element coupled between a reset node of the master-slave electronic fuse and the master latch; and

a slave latch having a slave-latch input coupled to an output of the master latch and a slave-latch node configured to receive a slave-latch signal,

wherein said master latch is configured to settle to a predetermined one of a first state and a second state following application of a reset signal to the reset node, and the slave latch is configured to latch the predetermined state of the master latch upon application of a slave-latch signal to the slave-latch node.

15. The master-slave electronic fuse of Claim 14, wherein the predetermined state of said master latch is affected by a memory value to which the nonvolatile memory element is programmed.

16. The master-slave electronic fuse of Claim 15, wherein said master latch comprises cross-coupled inverters.

17. The master-slave electronic fuse of Claim 15, wherein said nonvolatile memory element comprises a floating-gate transistor having a floating gate, an amount of charge on the floating gate determining said memory value.

18. The master-slave electronic fuse of Claim 17, wherein said nonvolatile memory element further comprises a first capacitor having a first plate in common with the floating gate of said floating-gate transistor.

19. The master-slave electronic fuse Claim 14, wherein said nonvolatile memory element comprises a nonvolatile memory element manufactured in a MOS fabrication process.

20. The master-slave electronic fuse of Claim 17, wherein said floating-gate transistor is MOS device.

21. The master-slave electronic fuse of Claim 14, wherein said nonvolatile memory element uses a mechanism selected from the group consisting of: magnetoresistive, ferroelectric, phase-change, and dielectric, for nonvolatile information storage.

22. The master-slave electronic fuse of Claim 17, wherein the amount of charge on the floating gate may be changed using Fowler-Nordheim tunneling.

23. The master-slave electronic fuse of Claim 17, wherein the amount of charge on the floating gate may be changed using hot-electron injection.

24. The master-slave electronic fuse of Claim 17, wherein the amount of charge on the first floating gate may be changed using direct tunneling.

25. The master-slave electronic fuse of Claim 17, wherein the amount of charge on the floating gate may be changed using hot-hole injection.

26. The master-slave electronic fuse of Claim 17, wherein the amount of charge on the floating gate may be changed using ultraviolet radiation.

27. The master-slave electronic fuse of Claim 17, wherein the nonvolatile memory element further comprises a second capacitor having a first plate in common with the floating gate of said floating-gate transistor.

28. The master-slave electronic fuse of Claim 14, further comprising a capacitive element coupled to an output of the master latch.

29. The master slave electronic fuse of claim 17, wherein the master latch is predisposed to settle into said first sate when a voltage of said floating gate is relatively high and into said second state when the floating gate voltage is relatively low.

30. The master-slave electronic fuse of claim 29, further comprising a capacitive element coupled between an output of the master latch and a fixed voltage source.

31. The master-slave electronic fuse of claim 29, wherein said master latch comprises cross-coupled inverters and wherein a first one of the cross-coupled inverters has at least one transistor with a gate-width-to-length ratio that is larger than a gate-width-to-length ratio of at least one of the transistors of a second one of said cross-coupled inverters.

32. The master-slave electronic fuse of claim 29, wherein said master latch comprises cross-coupled inverters and wherein a first one of the cross-coupled inverters has at least one transistor with a channel doping level that is different from a channel doping level of at least one of the transistors of a second one of said cross-coupled inverters.

33. A master-slave electronic fuse, comprising:

a master fuse having a master latch, a first nonvolatile memory element coupled between a reset node of the master-slave electronic fuse and first node of the master latch, and a second nonvolatile memory element coupled between the reset node and a second node of the master latch;

a slave latch having a slave-latch input coupled to an output of the master latch and a slave-latch node configured to receive a slave-latch signal,

wherein said master latch is configured to settle to a predetermined one of a first state and a second state following application of a reset signal to the reset node, and the slave latch is configured to latch the predetermined state of the master latch upon application of a slave-latch signal to the slave-latch node.

34. The master-slave electronic fuse of Claim 33, wherein the predetermined state of said master latch is affected by a first memory value associated with the first nonvolatile memory element.

35. The master-slave electronic fuse of Claim 34, wherein the predetermined state of the master latch is further affected by a second memory value associated with the second nonvolatile memory element.

36. The master-slave electronic fuse of Claim 34, wherein said first nonvolatile memory element comprises a first floating-gate transistor having a first floating gate, an amount of charge on the first floating gate determining said first memory value.

37. The master-slave electronic fuse of Claim 35, wherein said second nonvolatile memory element comprises a second floating-gate transistor having a second floating gate, an amount of charge on the second floating gate determining said second memory value.

38. The master-slave electronic fuse of claim 35, wherein said first nonvolatile memory element comprises a first floating-gate transistor having a first floating gate, an amount of charge on the first floating gate determining said first memory value and wherein said second nonvolatile memory element comprises a second floating-gate transistor having a second floating gate, and amount of charge on the second floating gate determining said second memory value.

39. The master-slave electronic fuse of Claim 38, wherein said first nonvolatile memory element further comprises a first capacitor having a first plate in common with the first floating gate of said first floating-gate transistor.

40. The master-slave electronic fuse of Claim 39, wherein said second nonvolatile memory element further comprises a second capacitor having a first plate in common with the second floating gate.

41. The master-slave electronic fuse of Claim 33, wherein said first and second nonvolatile memory elements comprise nonvolatile memory elements manufactured in a MOS fabrication process.

42. The master-slave electronic fuse of Claim 38, wherein at least one of said first and second floating-gate transistors are MOS devices.

43. The master-slave electronic fuse of Claim 33, wherein at least one of said first and second nonvolatile memory elements use a mechanism selected from the group consisting of: magnetoresistive, ferroelectric, phase-change, and dielectric, for nonvolatile information storage.

44. The master-slave electronic fuse of Claim 38, wherein the amount of charge on at least one of the first and second floating gates may be changed using Fowler-Nordheim tunneling.

45. The master-slave electronic fuse of Claim 38, wherein the amount of charge on at least one of the first and second floating gates may be changed using hot-electron injection.

46. The master-slave electronic fuse of Claim 38, wherein the amount of charge on at least one of the first and second floating gates may be changed using direct tunneling.

47. The master-slave electronic fuse of Claim 38, wherein the amount of charge on at least one of the first and second floating gates may be changed using hot-hole injection.

48. The master-slave electronic fuse of Claim 38, wherein the amount of charge on at least one of the first and second floating gates may be changed using ultraviolet radiation.

49. The master-slave electronic fuse of Claim 41, wherein the first nonvolatile memory element further comprises a third capacitor having a first plate in common with the first floating gate of said first floating-gate transistor.

50. The master-slave electronic fuse of Claim 49, wherein the second nonvolatile memory element further comprises a fourth capacitor having a first plate in common with the second floating gate of said second floating-gate transistor.

51. The master-slave electronic fuse of claim 38, wherein a first output of said master latches is capacitively coupled to a first source of a fixed voltage.

52. The master-slave electronic fuse of claim 51, wherein a second output of said master latches is capacitively coupled to a second source of a fixed voltage.

53. The master-slave electronic fuse of claim 52, wherein said first source of a fixed voltage and said second source of a fixed voltage are the same.

54. The master-slave electronic fuse of claim 38, wherein the master latch is predisposed to settle into one of said first and second states in response to said first and second memory values.

55. The master-slave electronic fuse of claim 54, further comprising a capacitive element coupled between an output of the master latch and a fixed voltage source.

56. The master-slave electronic fuse of claim 54, wherein said master latch comprises cross-coupled inverters and wherein a first one of the cross-coupled inverters has at least one transistor with a gate-width-to-length ratio that is larger than a gate-width-to-length ratio of at least one of the transistors of a second one of said cross-coupled inverters.

57. The master-slave electronic fuse of claim 54, wherein said master latch comprises cross-coupled inverters and wherein a first one of the cross-coupled inverters has at least one transistor with a channel doping level that is different from a channel doping level of at least one of the transistors of a second one of said cross-coupled inverters.

58. A master-slave electronic fuse, comprising:

a master fuse having a logic-gate element with a reset node and a nonvolatile memory element; and

a slave latch having a slave latch input coupled to an output of the master fuse and a slave latch node configured to receive a slave latch signal,

wherein said logic-gate element is configured to settle to a predetermined one of a first state and a second state following application of a reset signal to the reset node, and the slave latch is configured to latch the predetermined state of the logic-gate element upon application of a slave latch signal to the slave latch node.

59. The master-slave electronic fuse of Claim 58, wherein the predetermined state of said logic-gate element is affected by a memory value associated with the nonvolatile memory element.

60. The master-slave electronic fuse of Claim 59, wherein said nonvolatile memory element comprises a floating-gate transistor having a floating gate, an amount of charge on the floating gate determining said memory value.

61. The master-slave electronic fuse Claim 60, wherein said nonvolatile memory element further comprises a first capacitor having a first plate in common with the floating gate of said floating-gate transistor.

62. The master-slave electronic fuse Claim 58, wherein said nonvolatile memory element comprises a nonvolatile memory element manufactured in a MOS process.

63. The master-slave electronic fuse of Claim 60, wherein said floating-gate transistor is a MOS devices.

64. The master-slave electronic fuse of Claim 58, wherein said nonvolatile memory element uses a mechanism selected from the group consisting of: magnetoresistive, ferroelectric, phase-change, and dielectric, for nonvolatile information storage.

65. The master-slave electronic fuse of Claim 60, wherein the amount of charge on the floating gate may be changed using bidirectional Fowler-Nordheim tunneling.

66. The master-slave electronic fuse of Claim 60, wherein the amount of charge on the floating gate may be changed using Fowler-Nordheim tunneling.

67. The master-slave electronic fuse of Claim 60, wherein the amount of charge on the floating gate may be changed using hot-electron injection.

68. The master-slave electronic fuse of Claim 60, wherein the amount of charge on the floating gate may be changed using direct tunneling.

69. The master-slave electronic fuse of Claim 60, wherein the amount of charge on the floating gate may be changed using hot-hole injection.

70. The master-slave electronic fuse of Claim 60, wherein the amount of charge on the floating gate may be changed using ultra violet radiation exposure.

71. The master-slave electronic fuse of Claim 61, wherein the nonvolatile memory element further comprises a second capacitor having a first plate in common with the floating gate of said floating-gate transistor.

72. The master-slave electronic fuse of claim 60, wherein the logic-gate element is predisposed to settle into said first state when a voltage of said floating gate is relatively high and into said second state when the floating gate voltage is relatively low.